

WHAT IS CLAIMED IS:

1 1. A non-volatile semiconductor device comprising:
2 a semiconductor substrate;
3 source and drain regions in said substrate separated by
4 a channel region;

5 a gate comprising a layer of polycrystalline silicon of
6 conductivity type different from that of said source and drain
7 regions; and

8 a multilayer gate dielectric between said gate and said
9 channel region comprising a charge storage layer having
10 alterable charge storage properties by application of an
11 electric field and having a dielectric thickness equivalent to
12 that of a layer of silicon dioxide that is less than about 170
13 angstroms.

2. The device of claim 1 wherein said gate further comprises
a layer of refractory silicide.

3. The device of claim 1 wherein said gate contains as few as
 $10^{11}/\text{cm}^3$ electrically active atoms of doping material.

4. The device of claim 3 wherein said conductivity types
comprise a doping material selected from the group consisting
of antimony, boron, phosphorus and arsenic.

5. The device of claim 1 wherein said source and drain regions
are doped primarily N-type and said gate is doped P-type.

6. The device of claim 1 wherein said source and drain regions
are doped primarily P-type and said gate is doped N-type.

1 7. The device of claim 1 wherein said multilayer gate
2 dielectric further comprises a second dielectric material
3 layer between said charge storage layer and said channel.

1 8. The device of claim 7 wherein said second dielectric
2 material layer comprises silicon dioxide.

1 9. The device of claim 7 wherein said multilayer gate
2 dielectric further comprises a third dielectric material layer
3 between said charge storage layer and said gate.

1 10. The device of claim 9 wherein said third dielectric
2 material layer comprises silicon dioxide.

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1 16. The device of claim 1 wherein said charge storage layer
2 comprises a material selected from the group consisting of
3 silicon nitride, silicon oxynitride, silicon-rich silicon
4 dioxide, and ferroelectric materials.

1 17. The device of claim 1 wherein said substrate has a first
2 conductivity type and said source and drain regions are
3 semiconductor regions of a second conductivity type.

1 18. The device of claim 1 wherein said substrate has a first
2 conductivity type and said source and drain regions are
3 semiconductor regions of a first conductivity type; and

4 wherein said non-volatile memory device further comprises
5 a first well region of a second conductivity type formed in
6 said substrate as to surround at least said source and drain
7 regions and said channel region.

1 19. The device of claim 1 wherein said substrate has a first
2 conductivity type and said source and drain regions are
3 semiconductor regions of a second conductivity type; and

4 wherein said non-volatile memory device further comprises
5 a first well region of a first conductivity type formed in
6 said substrate as to surround at least said source and drain
7 regions and said channel region; and

8 wherein said non-volatile memory device further comprises
9 an additional second well region of the second conductivity
10 type formed in said substrate as to surround at least said
11 first well region.

1 20. The device of claim 1 wherein said channel region
2 comprises a buried channel.

1 21. The device of claim 1 wherein said channel region
2 comprises a depletion channel.

1 22. A non-volatile semiconductor device comprising:

2 a semiconductor substrate;

3 source and drain regions in said substrate separated by
4 a channel region having a channel length less than about 0.7
5 microns;

6 a gate comprising a layer of polycrystalline silicon of
7 conductivity type different from that of said source and drain
8 regions; and

9 a multilayer gate dielectric between said gate and said
10 channel region comprising a charge storage layer having
11 alterable charge storage properties by application of an
12 electric field.

13 23. The device of claim 22 wherein said gate further comprises
14 a layer of refractory silicide.

15 24. The device of claim 22 wherein said gate contains more
16 than $10^{11}/\text{cm}^3$ electrically active atoms of doping material.

17 25. The device of claim 24 wherein said conductivity types
18 comprise a doping material selected from the group consisting
19 of antimony, boron, phosphorus and arsenic.

20 26. The device of claim 22 wherein said source and drain
21 regions are doped primarily N-type and said gate is doped P-
22 type.

23 27. The device of claim 22 wherein said source and drain
24 regions are doped primarily P-type and said gate is doped N-
25 type.

1 28. The device of claim 22 wherein said multilayer gate
2 dielectric further comprises a second dielectric material
3 layer between said charge storage layer and said channel.

1 29. The device of claim 28 wherein said second dielectric
2 material layer comprises silicon dioxide.
3

4 30. The device of claim 28 wherein said multilayer gate
5 dielectric further comprises a third dielectric material layer
6 between said charge storage layer and said gate.

1 31. The device of claim 30 wherein said third dielectric
2 material layer comprises silicon dioxide.

3 32. The device of claim 30 wherein said third dielectric
4 material layer comprises a three layered structure of a layer
5 of silicon dioxide, on a layer of silicon nitride on yet
6 another layer of silicon dioxide.

1 33. The device of claim 22 wherein said charge storage layer
2 comprises a floating gate.

3 34. The device of claim 33 wherein said floating gate
4 comprises polycrystalline silicon.
5

6 35. The device of claim 22 wherein said charge storage layer
1 comprises a dielectric material capable of trapping charge
2 carriers.
3

1 36. The device of claim 22 wherein said charge storage layer
2 comprises a dielectric material capable of trapping charge
3 polarization.

1 37. The device of claim 22 wherein said charge storage layer
2 comprises a material selected from the group consisting of
3 silicon nitride, silicon oxynitride, silicon-rich silicon
4 dioxide, and ferroelectric materials.

1 38. The device of claim 22 wherein said substrate has a first
2 conductivity type and said source and drain regions are
3 semiconductor regions of a second conductivity type.

1 39. The device of claim 22 wherein said substrate has a first
2 conductivity type and said source and drain regions are
3 semiconductor regions of a first conductivity type; and

4 wherein said non-volatile memory device further comprises
a first well region of a second conductivity type formed in
said substrate as to surround at least said source and drain
regions and said channel region.

1 40. The device of claim 22 wherein said substrate has a first
2 conductivity type and said source and drain regions are
3 semiconductor regions of a second conductivity type; and

4 wherein said non-volatile memory device further comprises
5 a first well region of a first conductivity type formed in
6 said substrate as to surround at least said source and drain
7 regions and said channel region; and

8 wherein said non-volatile memory device further comprises
9 an additional second well region of the second conductivity
10 type formed in said substrate as to surround at least said
11 first well region.

1 41. The device of claim 22 wherein said channel region
2 comprises a buried channel.

1 42. The device of claim 22 wherein said channel region
2 comprises a depletion channel.

1 43. A non-volatile semiconductor device having source and
2 drain regions of first conductivity type in said substrate
3 separated by a channel region of length less than about 0.7
4 microns, comprising:

5 a gate comprising a layer of polycrystalline silicon of
6 second conductivity type different from that of said first
7 conductivity type; and

8 a multilayer gate dielectric between said gate and said
9 channel region comprising a charge storage layer having
10 alterable charge storage properties by application of an
11 electric field.

12 44. The non-volatile semiconductor device of claim 43 wherein
13 said gate dielectric has a dielectric thickness equivalent to
14 that of a layer of silicon dioxide that is less than about 170
15 angstroms.

16 45. The device of claim 43 wherein said gate further comprises
17 a layer of refractory silicide.

1 46. The device of claim 43 wherein said source and drain
2 regions are doped primarily N-type and said gate is doped P-
3 type.

1 47. The device of claim 43 wherein said source and drain
2 regions are doped primarily P-type and said gate is doped N-
3 type.

1 48. The device of claim 43 wherein said charge storage layer
2 comprises a floating gate.

1 49. A method for making a non-volatile semiconductor device
2 comprising:

3 *Sub* forming a multilayer gate dielectric having a charge
4 *K3* storage layer with alterable charge storage properties by
5 application of an electric field, and having a dielectric
6 thickness equivalent to that of a layer of silicon dioxide
7 that is less than about 170 angstroms;

8 forming a gate comprising polycrystalline silicon of
9 first conductivity type on said gate dielectric; and

10 forming source and drain regions separated by a channel
11 region in a semiconductor substrate, said source and drain
12 regions having a second conductivity type different from said
13 first dielectric type.

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